AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 2, line 17, with the following rewritten paragraph:

1   The present invention achieves these technical advantages by
2 ascertaining and analyzing events that are guaranteed to be present in all
3 SONET/SDH data streams. A1 and A2 framing bytes occur at 125
4 microseconds intervals in all SONET/SDH signals. The transitions of these bits
5 in the framing bytes represent the minimum transition intervals of the received
6 data. The present invention examines this transition interval to measure the bit
7 data rate and determine the operating frequency of the received data. A series
8 of flip-flops are used to clock in the A1 and A2 framing bytes at the maximum
9 possible data bit-rate. A set of static combinational byte-logic circuits are used to
10 detect specific data-bit patterns which appear in the A1 and A2 SONET framing
11 bytes. Each combinational circuit looks for a pattern occurring at a specific
12 communication rate. Flip-flops ~~Latches~~ capture the pulses that are generated by
13 the combinational circuits each time that the pattern is detected. After a
14 sufficient predetermined time has passed, the output of the capturing flip-flops
15 ~~latches~~ indicates which bit-rates have been detected. A multi-rate transceiver
16 chip is then responsively set to operate at the highest rate detected.

Please replace the paragraph beginning at page 3, line 6, with the following rewritten paragraph:

1   Figure 1 is a block diagram overview of a SONET communication link
2 having a multi bit-rate SONET transceiver at each end;

3   Figure 2 illustrates the timing of the A1 and A2 framing bytes occurring at
4 125 microsecond intervals;

5   Figure 3 is a schematic of a set of flip-flops used to serially clock in the

6   arriving ~~framing byte~~ data. The ~~and which~~ flip-flops are clocked at the fastest bit-

7   rate possible;

8   Figure 4 is a schematic of the rate detect circuit <u>50</u> illustrated in Figure 3

9   according to the present invention including combinational circuits detecting data

10   patterns to ascertain the bit-rate of the incoming data; and

11   <u>Figures 5A, 5B and 5C together show</u> ~~Figure 5 is~~ a schematic of a second

12   embodiment of the invention including a rate detection circuit adapted to analyze

13   parallized data.

        Please replace the paragraph beginning at page 4, line 17, with the
following rewritten paragraph:

1   These bits are transmitted unscrambled so that these framing bits

2   represent the minimum transition intervals of the data corresponding to the

3   maximum data bit-rate or data frequency. The present invention examines these

4   framing and other bytes to quickly and accurately measure the data bit-rate and

5   determine the operating frequency of the incoming received data. The "101" and

6   "010" bit sequence portion of these A1 and A2 framing bytes are searched, the

7   presence of which when detected is indicative of and corresponds to a <u>maximum</u>

8   ~~minimum~~ bit-rate.

        Please replace the paragraph beginning at page 4, line 23, with the
following rewritten paragraph:

1   Referring now to Figure 3, there is illustrated at 30 an automatic bit-rate

2   detection circuit comprising a portion of transceiver 14. A set of <u>flip-flops</u> ~~flip-flop~~

3   ~~devices~~ 32 ~~that~~ are used to serially clock in the arriving bits of the A1 and A2

4   framing bytes. This arriving framing bits are provided to input 34 of the first flip-

5   flop 32 shown at left. The maximum clock rate ~~(clk)~~ of clock 36, in this example,

6   operating at 2.488 <u>GHz/s</u> ~~Gb/s~~, clocks the framing bits from input 34 through the

7 set of flip-flops 32. If It the actual incoming data bit-rate is the maximum data

8 rate and clock speed, i.e. 2.488 Gb/s Gbls, each bit will be clocked into one flip-

9 flop 32. If the actual incoming data bit-rate is ½ of the maximum data rate and

10 clock speed, i.e. 1.244 Gb/s, each bit will be clocked into two (2) flip-flops 32.

11 Likewise, if the incoming data bit-rate is received at ¼ the maximum data rate,

12 i.e. .622 Gb/s, each bit of the framing data will be clocked into four (4) flip-flops

13 32.

        Please replace the paragraph beginning at page 5, line 7, with the
following rewritten paragraph:

1   The output of each flip-flop 32 is provided on data lines 40 to a rate

2 detect circuit 50 according to the present invention. These data bits are provided

3 in parallel to the logic circuit 50 and are represented as data bits do(1), do(3),

4 do(4), do(5), do(6) and do(7). Initially, the flip-flops 32 are in the reset condition.

        Please replace the paragraph beginning at page 5, line 11, with the
following rewritten paragraph:

1   Referring now to Figure 4, there is illustrated in more detail the rate detect

2 circuit 50 shown in Figure 3. Shown in Figure 4 is a plurality of combinational

3 logic circuits each having inputs connected to a unique set of nodes between flip-

4 flops 32 and receiving the clocked output data from the respective flip-flops 32 in

5 Figure 3. Flip-flops 76, 86 and 96 are reset before the evaluation begins. The D

6 inputs of flip-flops 76, 86 and 96 are set high so that the first time these flip-flops

7 get clocked, their Q outputs go high. Shown at 70 is a first combinational logic

8 group having a pair of 4-input NAND gates 72 receiving a first set of data bits

9 data do(7), do(6), do(5) and do(4). The NAND gates are logically connected to

10 look for a 1010 or 0101 data pattern in the framing bytes A1 and A2. If either of

11 these data bit patterns appear, the received framing data clocked into circuit 50

12   is determined to must be ~~switching~~ at the same rate as the clock 36, i.e. 2.488

13   Gb/s. Accordingly, and responsively, the combinational circuit 70 generates a

14   logic 1 pulse at output 74 thereof, and a first D flip-flop shown at 76 will have a

15   logic low at its inverting output 4.

Please replace the paragraph beginning at page 5, line 22, with the following rewritten paragraph:

1   Similarly, a second combinational logic circuit shown at 80 has a pair of 3-

2   input NAND gates 82 looking at a second set of input data bits do(7), do(5), and

3   do(3) and looking for a 101 or 010 data-bit pattern ~~in the framing bytes A1 and~~

4   ~~A2~~. If either of these data bit patterns appears, the incoming framing bytes data

5   bits are determined to possibly, but not necessarily, be switching at ½ the

6   maximum clock rate, i.e. 1.244 Gb/s. Accordingly, this combinational logic circuit

7   80 generates a logic at output 84, 1 pulse that will cause corresponding a D flip-

8   flop shown at 86 to have a low value at its inverting output.

Please replace the paragraph beginning at page 6, line 3, with the following rewritten paragraph:

1   Shown at 90 is a third combinational logic circuit having a pair of 4-input

2   NAND logic gates 92 looking at third set of input data bits do(7), do(5), do(3) and

3   do(1) and looking for a data bit pattern 1001 or 0110. If this data bit sequence is

4   detected, it is determined that the input data ~~rate of the framing data A1 and A2~~

5   may be switching at 1/4 the maximum clock rate i.e. .622 Gb/s. Accordingly, this

6   combinational circuit 90 generates a logic 1 pulse at or about 94 that will cause a

7   D flip-flop 96 to have a low value at its inverting output.

Please replace the paragraph beginning at page 7, line 1, with the following rewritten paragraph:

1   Knowing the predetermined data bit patterns of the bits in the A1 and A2

2   framing bytes, which again, is common in all SONET signals regardless of the

3   data communication bit rate, allows the logic circuitry 50 to sample <u>the serial</u> ~~this~~

4   data to search for the "101" or "010" bit sequence at the highest possible data bit

5   rate, and thus ascertain the data-bit-rate. The D flip-flops 32 provide nodes

6   which allow the combinational circuit to sample data of the flip-flops 32 and to

7   determine the data bit-rate. For instance, ~~with regards to the framing byte A1,~~ if

8   data is received at ½ the maximum data rate, every bit of the framing byte will be

9   clocked into two (2) flip-flops 32. ~~This is the same for the bits of the A2 framing~~

10   ~~byte.~~

        Please replace the paragraph beginning at page 7, line 9, with the
following rewritten paragraph:

1   Similarly, if incoming ~~framing~~ data is received at ¼ the maximum data

2   rate, i.e., .622 Gb/s in this example, each ~~framing~~ bit of the <u>data stream</u> ~~framing~~

3   ~~bytes~~ will be clocked into four of the flip-flops 32. Thus, <u>the maximum data rate</u>

4   <u>can be ascertained by searching for the "010" or "101" pattern which fits into the</u>

5   <u>smallest number of flip-flops 32.</u> ~~for instance, the first bit being a logic "1" of~~

6   ~~framing byte A1 is clocked through the first four D flip-flops 32 such that a logic 1~~

7   ~~is provided at outputs do(7), do(6), do(5) and do(4). However, the logic circuit 56~~

8   ~~clocks (samples) this data in at the maximum data rate of 2.44 Gb/s. The~~

9   ~~framing bits of both framing bytes are eventually clocked through the flip-flops~~

10   ~~32, and the combinational logic circuits sample and detect the bit sequence,~~

11   ~~where the "101" or "010" bit patterns of the framing bytes are screened for the~~

12   ~~entire framing bytes. After 250 microseconds have past, again, sufficient for at~~

13   ~~least one of the SONET frame bytes to have been received and clocked through~~

14   ~~the flip-flops 32, the outputs at the respective combination logic circuits 70, 80~~

15   ~~and 90 are provided to the combinational circuits 76, 86 and 96, respectively,~~

16   ~~and the combinational circuit 100.~~

Please replace the paragraph beginning at page 7, line 21, with the following rewritten paragraph:

1   Referring now to <u>Figures 5A, 5B and 5C</u> ~~Figure 5~~, there is shown a

2   schematic of a circuit <u>500 (portions 500a, 500b and 500c, respectively)</u> that can

3   detect a data rate of parallized data. By way of illustration, but without any

4   intended limitation, data parallelized into a 4-bit bus will be discussed for clarity

5   and understanding of this embodiment.

Please replace the paragraph beginning at page 8, line 1, with the following rewritten paragraph:

1   The data comes into <u>the portion 500c of</u> this circuit <u>500</u> ~~100~~ in the form of

2   a 4-bit bus. The task is to extract the "101" or "010" from the framing bytes of

3   this data stream. The clock that drives these flip-flops no longer needs to be at

4   the highest possible frequency of the data stream we want to detect. Rather, the

5   clock CLK, in this example, runs at ¼ the highest possible data rate to be

6   detected. The limitation is that, now, the "101" or "010" bit pattern could be

7   hiding in one of several positions.

Please replace the paragraph beginning at page 8, line 7, with the following rewritten paragraph:

1   Looking at the case for the highest incoming rate, if we represent the data

2   in serial manner, the bits would have come in as:

3   A3 A2 A1 A0 B3 B2 B1 <u>as labeled in Figure 5c</u> ~~← direction of data~~

4   ~~stream~~

5   Note: this data stream matches the Q output label of the flip-flops.

Please replace the paragraph beginning at page 8, line 13, with the following rewritten paragraph:

1   Thus, the <u>mechanism shown in Figures 5A, 5B and 5C</u> ~~combinational~~
2   ~~logic 102~~ needed to detect the "101" or "010" bit pattern becomes more
3   complicated, as illustrated.

Please replace the paragraph beginning at page 8, line 15, with the following rewritten paragraph:

1   For the lower bit-rate cases, such as a received data bit-rate at ½ max
2   rate data rate, the bit pattern we look for is "110011" or "001100". Since there
3   are consecutive 0's and 1's the bits we observe get reduced, and this is taken
4   advantage of in the circuit ~~shown on Figure 5~~.